High-Speed Board Designs

January 1998, ver. 2 Application Note 75

Introduction

To create a successful high-speed printed circuit board (PCB), you must integrate the device(s), PCB(s), and other elements into the design. Altera® devices have fast I/O pins, with fall times that can be as low as 1 to 3 ns. Because a fast slew rate can contribute to noise generation, signal reflection, cross-talk, and ground bounce, your designs must:

- Filter and evenly distribute power to all devices to reduce noise
- Terminate signal and transmission lines to diminish signal reflection
- Minimize cross-talk between parallel traces
- Reduce the effects of ground bounce

Power Filtering & Distribution

You can dramatically reduce system noise by providing a clean, evenly distributed power to V_{CC} on all boards and devices.

Filtering Noise

To diminish the low-frequency (< 1 kHz) noise caused by the power supply, you must filter the noise on the power lines at the point where the power connects to the PCB, and where it connects to each device. Altera recommends placing a 100-µF electrolytic capacitor immediately adjacent to the location where the power supply lines enter the PCB. If you use a voltage regulator, place the capacitor immediately after the final stage that provides the V_{CC} signal to the device(s). Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.

The components on the PCB add high-frequency noise to the power plane. To filter high-frequency noise at the device, Altera recommends placing decoupling capacitors as close as possible to each V_{CC} and ground pair.

See the *Operating Requirements for Altera Devices Data Sheet* in this data book for more information on bypass capacitors.

Distributing Power

Power distribution also has an impact on system noise. Power can be distributed throughout the PCB with either a power bus network or power planes.

The least expensive method is a power bus network, which consists of two or more wide, metal traces that carry V_{CC} and ground to the devices. Usually used on two-layer PCBs, power buses provide an inexpensive method of supplying power. The trace widths, which should be as wide as possible, are limited by the density of the PCB. Power buses have significant DC resistance; the last element on the bus may receive V_{CC} power that is degraded by as much as 0.5 V.

Altera recommends using power planes to distribute power. Power planes are used on multi-layer PCBs and consist of two or more metal layers that carry V_{CC} and ground to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains V_{CC} and distributes it equally to all devices, while also providing very high current-sink capability, noise protection, and shielding for the logic signals on the PCB.

Signal & Transmission Line Termination

Having established the PCB power network, you must consider the layout of the devices and traces. Fast edge rates contribute to noise, cross-talk, and ground bounce to varying degrees, depending on the PCB construction material.

Each PCB substrate has a different relative dielectric constant (E_r) that measures the effect of an insulator on the capacitance of a conductor pair compared to the capacitance of the conductor pair in a vacuum. The type of substrate used determines the length at which the signal traces must be handled as transmission lines. Table 1 lists E_r values for various dielectric materials.

Table 1. Relative Dielectric Constants

Material	E_r
Air	1.0
PTFE/glass	2.2
Rogers RO 2800	2.9
CE/goreply	3.0
BT/goreply	3.3
CE/glass	3.7
Silicon dioxide	3.9
BT/glass	4.0
Polymide/glass	4.1
FR-4/glass	4.1
Glass cloth	6.0
Alumina	9.0

The following equation shows how the relative dielectric constant (E_r) of the material determines the velocity (V_P) at which signals may flow. The constant (C) equals 3×10^8 m / s or 30 cm / ns:

$$V_P = \frac{C}{\sqrt{E_r}}$$

The propagation delay (PD) can be calculated for a given length (l) where:

$$PD = \frac{l}{V_P}$$

When driving a line, the circuit can be viewed as either a lumped or distributed circuit. The determining factor is when the signal edge rate ($\mathbf{t_R}$) is greater than four times the PD:

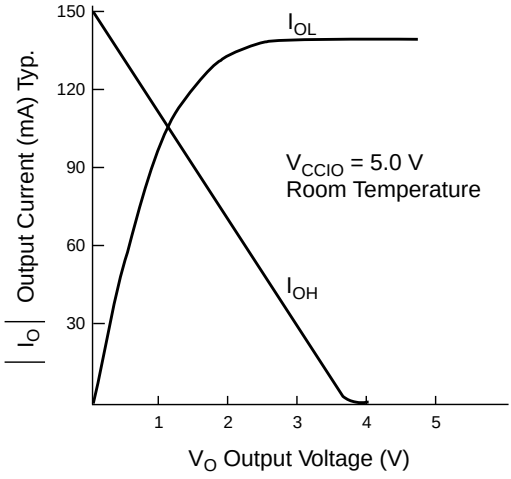
Lumped: $\mathbf{t_R} < 4 \times PD$

Distributed: $\mathbf{t_R} > 4 \times PD$

Distributed circuits are modeled as transmission lines which exhibit ringing, overshoot, and undershoot. In contrast, lumped circuits can be modeled where the voltage is the same across the line. Some lumped systems do exhibit ringing, especially those which have large inductance, like those which are point-to-point wired.

An Altera device's signal edge rate at the rising edge is a function of the capacitance that is driven by the device. You can estimate this signal edge rate if you know the device's capacitive load. Altera device family data sheets include output drive characteristics graphs that show the voltage / current relationship of the output drives. You can derive an equation for signal edge rate at the rising edge as a function of capacitance using these output drive characteristics graphs. Figure 1 shows the output drive characteristics for the MAX® 7000 device family, which is also used to determine the signal edge rate.

Figure 1. Output Drive Characteristics of MAX 7000 Devices



The falling edge, represented by the I_{OL} curve, has a sharper edge rate and is more susceptible to transmission line effects. The curve is roughly linear when it goes from 10% to 90%. The following linear approximation is used:

$$I_{OL} = 0.06\ V_O$$

Solving the charging capacitor equation for time (t) yields the following equations:

$$\frac{\partial V}{\partial t} = \frac{I_O}{C}$$

$$\partial t = \frac{C}{I_O}(\partial V)$$

Substituting the equation above for I_{OL} yields the following equation:

$$\partial t = \frac{C}{(0.06V)}(\partial V)$$

Integrating and solving the integral from 10% to 90% yields the following signal edge rate ($\mathbf{t_F}$) equation for the falling edge:

$$\mathbf{t_F} = C\frac{1}{0.06} \times \ln(0.06V)\Big|_{0.2}^{2.1} = -34.52 - (-73.71) = 39.19 \times C$$

To calculate output delay time, you must first determine the fall time of the specified load. To drive a 35-pF load, the fall time would be:

$$\mathbf{t_F} = 39.19 \times (35 \times 10^{-12})\,\text{sec} = 1.37\ \text{ns}$$

Again, the propagation delay (PD) is the length (l) of the line divided by the velocity (V_P):

$$PD = \frac{l}{V_P}$$

By solving for length (l) using the equation below, you can calculate the length at which the line must be treated as a transmission line:

$$l > \frac{t_R \times C_O}{4\sqrt{E_R}} = \frac{(1.37 \times 10^{-9})(3 \times 10^{8})}{4\sqrt{4.1}} = 5.07 \text{ cm}$$

For example, when using a MAX 7000 device to drive a 35 pF load through a glass cloth substrate line that is greater than 4.96 cm, the line should be treated as a transmission line which can exhibit ringing, overshoot, and undershoot. The I_{OL} curve was estimated to have the faster edge rate, and therefore, it is prone to the transmission line effects. However, if I_{OH} has the faster edge rate, it would be more susceptible, and its linear approximation would be used to calculate the length (l).

In the example above, the MAX 7000 device has a normal slew rate and its V_{CCIO} is 5.0 V. If the slow slew rate logic option is turned on or I/O pins are connected to 3.3 V, the edge rate of the MAX 7000 device will be slower. If V_{CCIO} is connected to 3.3 V, the diagram of its output drive characteristics must be used to calculate $\mathbf{t_F}$.

If the slow slew rate option is turned on, then the new $\mathbf{t_F}$ will increase. The new $\mathbf{t_F}$ calculation is expressed as:

$\mathbf{t_F} = (t_{OD3} - t_{OD2}) + \mathbf{t_F}$ [calculated from the above equation for a normal slew rate]

For example, if a -10 device is used where t_{OD3} = 5.5ns and t_{OD1} = 1.5 ns, then $(t_{OD3} - t_{OD1})$ = (5.5 – 1.5) ns = 4 ns, and the new $\mathbf{t_F}$ for a slow slew rate can be calculated as shown below:

4 ns + 1.37 ns = 5.37 ns

With the slow slew rate option turned on, the new length (l) used to determine a transmission line is 19.89 cm.

Consult the appropriate device data sheet in this data book to see if a slow slew rate control affects both the rising and falling edge rates of the device you are using.

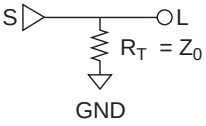
Impedance Matching & Termination Schemes

Mismatched impedance causes signals to reflect back and forth, and up and down the line, which in turn causes ringing at the load. To eliminate reflections, the impedance of the source (Z_S) must equal the impedance of the trace (Z_0), as well as the load (Z_L).

The load impedance is typically much higher than the line impedance, which is higher than the source impedance. On an unmatched transmission line, a signal reflects 100% at the load and approximately 80% at the source, bouncing back and forth until it dies out. To reduce signal reflection, you can match the impedance either at the load (Z_L) or at the source (Z_S) to the line impedance (Z_0). You can match the impedance by adding an impedance in parallel with the load to reduce its input impedance.

Parallel termination diminishes the first reflection by matching the load impedance to the line impedance. The following examples show four parallel termination circuits. Altera recommends using either the Thevenin or resistor and capacitor (series-RC) scheme. For the matching to be effective, you must terminate each load, because any impedance mismatch will result in a signal reflection.

Simple Parallel Termination



In a simple parallel termination scheme, the terminating resistor (R_T) is equal to the line impedance. The placement of the termination resistor must be as close to the load as possible to be efficient. The current loading of this termination is highest at a high-output state. You can estimate the current load (I_L) with the following equation:

$$I_L = \frac{V_O}{R_T}$$

The driving voltage (V_O) can be calculated from the I_{OH} curve (refer to Figure 1 on page 524). The linear equation for I_{OH} is represented as:

$$I_{OH} = 0.15 - (0.038) \times V_O$$

$$V_O = \frac{(0.15 - I_{OH})}{0.038}$$

Therefore, we can calculate the current load for a 1.0 kΩ termination:

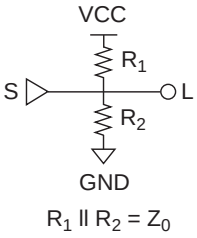
$$I_L = \frac{0.15 - I_{OH}}{0.038 \times 1,000} = \frac{0.15 - I_{OH}}{38}$$

When driving a high, $I_L = I_{OH}$, therefore:

$$I_L = \frac{0.15}{39} = 3.85\text{mA}$$

The current load should not exceed the DC operating conditions of a MAX 7000 device, 4 mA for I_{OH} and 12 mA for I_{OL}. In this case, the 3.85-mA current load is less than the maximum I_{OH} limit of 4 mA per output pin for MAX 7000 devices.

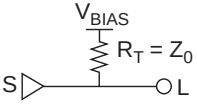
Thevenin Parallel Termination



$R_1 \parallel R_2 = Z_0$

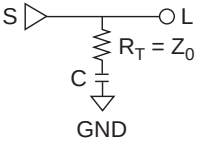
An alternative parallel termination scheme uses a Thevenin voltage divider. The terminating resistor is split between R_1 and R_2, which equal the line impedance when combined. Although this scheme reduces the current draw from the source device, it adds current drawn from the power supply because the resistors are tied between V_{CC} and ground.

Active Parallel Termination



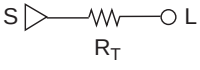
In an active parallel termination scheme, the terminating resistor ($R_T = Z_0$) is tied to a bias voltage (V_{BIAS}). The bias voltage is selected so that the output drivers are capable of drawing current from the high- and low-level signals. However, this scheme requires a separate voltage source that can sink and source currents to match the output transfer rates.

Series-RC Parallel Termination



In a parallel termination scheme, a resistor and capacitor (series-RC) network is used as the terminating impedance. The terminating resistor (R_T) is equal to Z_0; the capacitor must be greater than 100 pF. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of R_T does not have an impact on the driver.

Series Termination



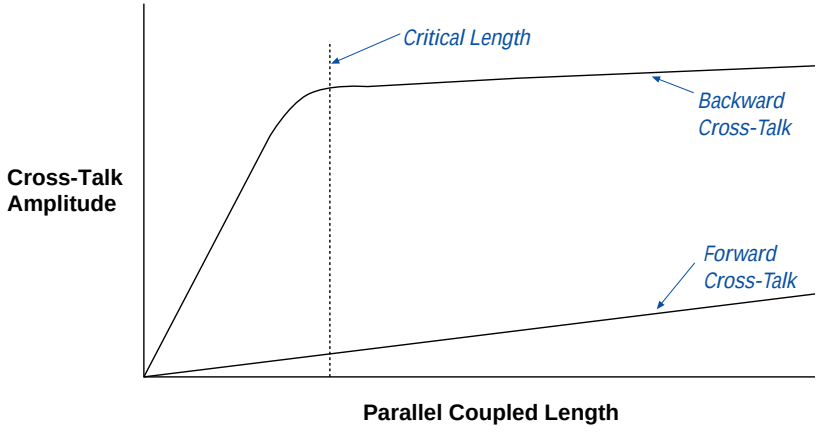
A series termination scheme matches the impedance at the signal source instead of matching the impedance at each load. Because the output impedance of Altera devices is low, you must add a series impedance to match the signal source to the line impedance.

On an unmatched line, the source eventually reduces the reflections; adding the series termination helps attenuate secondary reflections. The line impedance varies depending on the distribution of the load. Therefore, you cannot choose a single resistor value that applies to all conditions. Altera recommends using a 33-Ω series resistor to cover most impedances. This method requires only a single component at the source rather than multiple components at each load, but delays the signal path as it increases the RC time constant.

Cross-Talk

Cross-talk is the unwanted coupling of signals between parallel traces. Two types of cross-talk exist: forward (capacitive) and backward (inductive). Figure 2 illustrates the effect of each type of cross-talk as a function of the parallel length.

Figure 2. Cross-Talk as a Function of Parallel Length

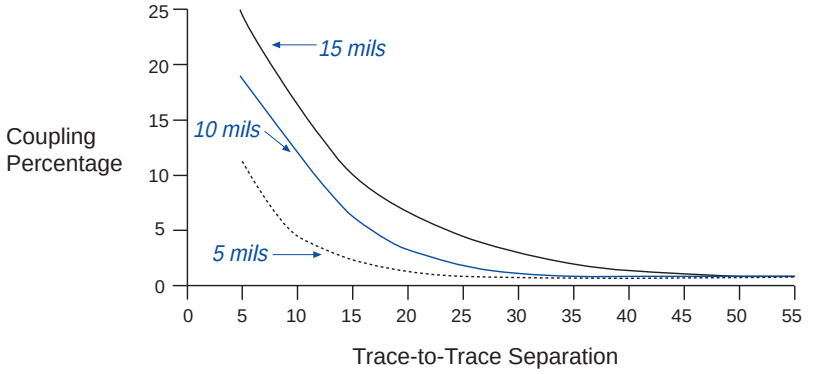


Forward cross-talk has the lesser effect between two traces. Two long running parallel traces will have a mutual capacitance between their two lines. When a voltage change is introduced into one trace, a capacitive effect on the other trace is produced, and this effect appears as a small positive pulse shaped like the derivative of the original voltage change.

Backward cross-talk, which has a more dramatic effect than forward cross-talk, occurs when the magnetic field from one trace induces a signal in a neighboring trace. In logic systems, the current flow through a trace is significant when the signals are switching or non-static. The magnetic fields created by switching currents induce the coupling transients.

You can dramatically reduce cross-talk by limiting the trace distance to 10 mils above the ground plane. Figure 3 shows the effect of trace height on trace-to-trace coupling.

Figure 3. Effect of Trace Height on Trace-to-Trace Coupling



Ground Bounce

As digital devices become faster, their output switching times decrease. Faster switching times cause higher transient currents in outputs as they discharge load capacitances. These higher currents, which are generated when multiple outputs of a device switch simultaneously from a logic high to a logic low, can cause a board-level phenomenon known as ground bounce.

Many factors contribute to ground bounce. Therefore, no standard test method allows you to predict its magnitude for all possible PCB environments. You can only test the device under a given set of conditions to determine the relative contributions of each condition and of the device itself. Load capacitance, socket inductance, and the number of switching outputs are the predominant factors that influence the magnitude of ground bounce in programmable logic devices.

Design Recommendations

Altera recommends that you take the following steps to reduce ground bounce:

- Turn on the slow slew rate logic option for FLEX® 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000A, and MAX 7000 designs
- Limit load capacitance by buffering loads with an external device such as the 74244 IC bus driver, or by reducing the number of devices that drive the bus
- Eliminate sockets whenever possible
- Reduce the number of outputs that can switch simultaneously and / or distribute them evenly throughout the device
- Move switching outputs close to a package ground pin.
- Create a programmable ground next to your switching pins
- Eliminate pull-up resistors, or use pull-down resistors

- Use multi-layer PCBs that provide separate V_{CC} and ground planes
- Add 10- to 30-Ω resistors in series to each of the switching outputs to limit the current flow into each of the outputs
- Create synchronous designs that will not be affected by momentarily switching pins

Search for "Slow Slew Rate" in MAX+PLUS® II Help for more information about this logic option.

These design recommendations, many of which are described in detail later in this application note, should help you create effective high-speed logic designs that operate over a wide range of PCB conditions.

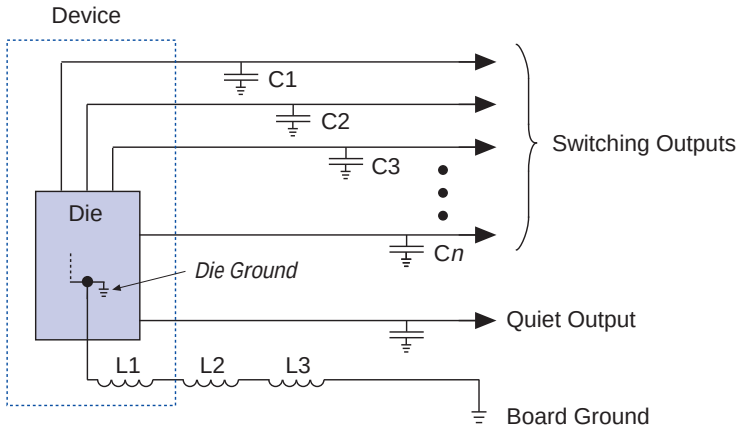
Analyzing Ground Bounce

Figure 4 shows a simple model for analyzing ground bounce. The external components driven by the device appear to that device as capacitive loads (C1 to C*n*). These capacitive loads store a charge that is determined by the following equation:

charge (Q) = [voltage (V) × capacitance (C)]

Thus, the charge increases as the voltage and / or load capacitance increases.

Figure 4. Ground Bounce Model



The environment and ground path of a device have intrinsic inductances (shown in Figure 4 as L1, L2, and L3). L1 is the inductance of the bond wire from the device's die to its package pin, and of the pin itself. L2 is the inductance of the connection mechanism between the device's ground pin and the PCB. This inductance is greatest when the device is connected to the PCB through a socket. L3 is the inductance of the PCB trace between the device and the PCB location where the power supply's reference ground is connected.

Ground bounce occurs when multiple outputs switch from high to low. The transition causes the charge stored in the load capacitances to flow into the device. The sudden rush of current ($\partial i / \partial t$) exits the device through the inductances (L) to board ground, generating a voltage (V) determined by the equation $V = L \times (\partial i / \partial t)$. This voltage difference between board ground and device ground causes the relative ground level for low or quiet outputs to temporarily rise or bounce. Although the rush of current is brief, the magnitude of the bounce can be large enough to trigger other devices on the PCB.

In synchronous designs, ground bounce is less often a problem because synchronous outputs have enough time to settle before the next clock edge. Also, synchronous circuits are not as likely to be falsely triggered by a voltage spike on a quiet output.

Ground bounce is affected differently by capacitive loading on the switching outputs and quiet outputs.

Switching Outputs

When the capacitive loading on the switching outputs increases, the amount of charge available for instantaneous switching increases, which in turn increases the magnitude of ground bounce. Depending on the device, ground bounce increases with capacitive loading until the loading is approximately 100 pF per device output. At this point, the device output buffers reach their maximum current-carrying capacity and inductive factors become dominant.

One method of reducing the capacitive load, and consequently ground bounce, is to connect the device's switching outputs to a bus driver integrated circuit (IC). The outputs of the bus driver IC drive the heavy capacitive loads, reducing the loading on the device, thus minimizing ground bounce for the device's quiet outputs.

Some bus applications use pull-up resistors to create a default high value for the bus. These resistors cause the load capacitances to charge up to the maximum voltage. Consequently, the driving device produces a higher level of ground bounce. Therefore, you should eliminate pull-up resistors in applications in which ground bounce is a concern, or design a bus logic that uses pull-down resistors instead.

The number of switching outputs also affects ground bounce. As the number of switching outputs increases, the total charge stored also increases. The total charge is equal to the sum of the stored charges for each switching output. Therefore, the amount of current that must sink to ground increases as the number of switching outputs increases. Ground bounce can increase by as much as 40 to 50 mV for each additional output that is switching.

To counteract these effects, Altera devices provide multiple VCC and GND pin pairs. You can reduce ground bounce by moving switching outputs close to a ground pin, and by distributing simultaneously switching outputs throughout the device.

Besides placing switching pins next to a ground pin, you can create a programmable ground pin by creating an output pin in your design that drives only ground. By connecting this output pin to ground on the board, the device ground will have another connection to the board ground, which helps reduce ground bounce.

Many Altera devices have slew rate options for the output drivers. Turning on the slow slew rate option for all or most of the drivers slows down the drivers, decreasing $\partial i / \partial t$ and reducing ground bounce.

To further reduce ground bounce, limit the number of outputs that can switch simultaneously in your design. For functions such as counters, you can use Gray coding as an alternative to standard sequential binary coding, since only one bit switches at a time.

In extreme cases, adding resistors (10 Ω to 30 Ω is usually adequate) in series to each of the switching outputs in a high-speed logic device can limit the current flow into each of the outputs, and thus reduce ground bounce to an acceptable level.

Quiet Outputs

An increase in capacitive loading on quiet outputs acts as a low-pass filter and tends to dampen ground bounce. Capacitive loading on a quiet output can reduce ground bounce by as much as 200 to 300 mV. However, an increase in capacitive loading on a quiet output can increase the noise seen on other quiet outputs when the capacitive-loaded pin does switch.

Minimizing Lead Inductance

Socket usage and PCB trace length are two elements of L2, the inductance of the connection mechanism between the device's ground pin and the PCB, shown in Figure 4 on page 530. Sockets can cause ground bounce voltage to increase by as much as 100%. You can often dramatically reduce the ground bounce on the PCB by eliminating sockets. The length of the PCB trace has a much smaller effect on ground bounce compared to sockets. For PCBs with a ground plane, the voltage drop across the inductance (L3) of the PCB trace between the device and the PCB location where other devices in the system reference ground is negligible, because L3 is significantly less than L2. The inductance in a 3-inch trace increases ground bounce for a quiet output by approximately 100 mV. Therefore, trace length should be kept to a minimum. As traces become longer, transmission line effects may cause other noise problems.

You can also reduce ground bounce due to PCB trace inductance by using multi-layer PCBs that provide separate V_{CC} and ground planes. Wire-wrapping the V_{CC} and ground supplies usually increases the amount of ground bounce. To reduce unwanted inductance, you should use low-inductance bypass capacitors between the V_{CC} supply pins and the board ground plane, as close to the package supply pins as possible. A standard decoupling capacitor (0.02 µF to 0.2 µF) used in parallel with a high-frequency decoupling capacitor (470 pF is a standard value) gives the best results.

References

Knack, Kella. ***Debunking High-Speed PCB Design Myths***. ASIC & EDA, Los Altos: James C. Uhl, July 1993.